

PG160-B02

8GB GDDR6, 256b, X16
Tall DVI-D + USB/DP + DP + HDMI/DP + DP

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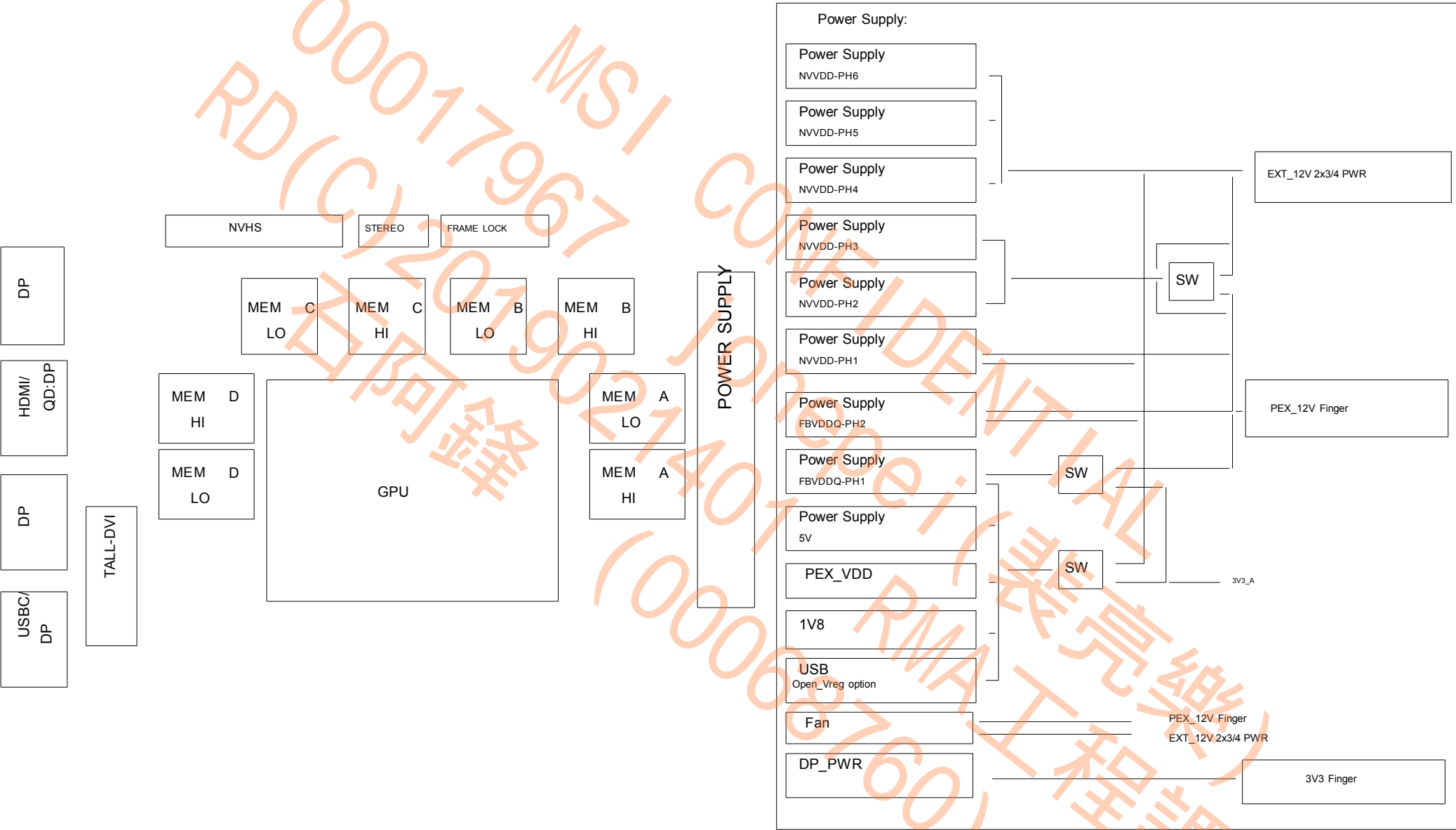
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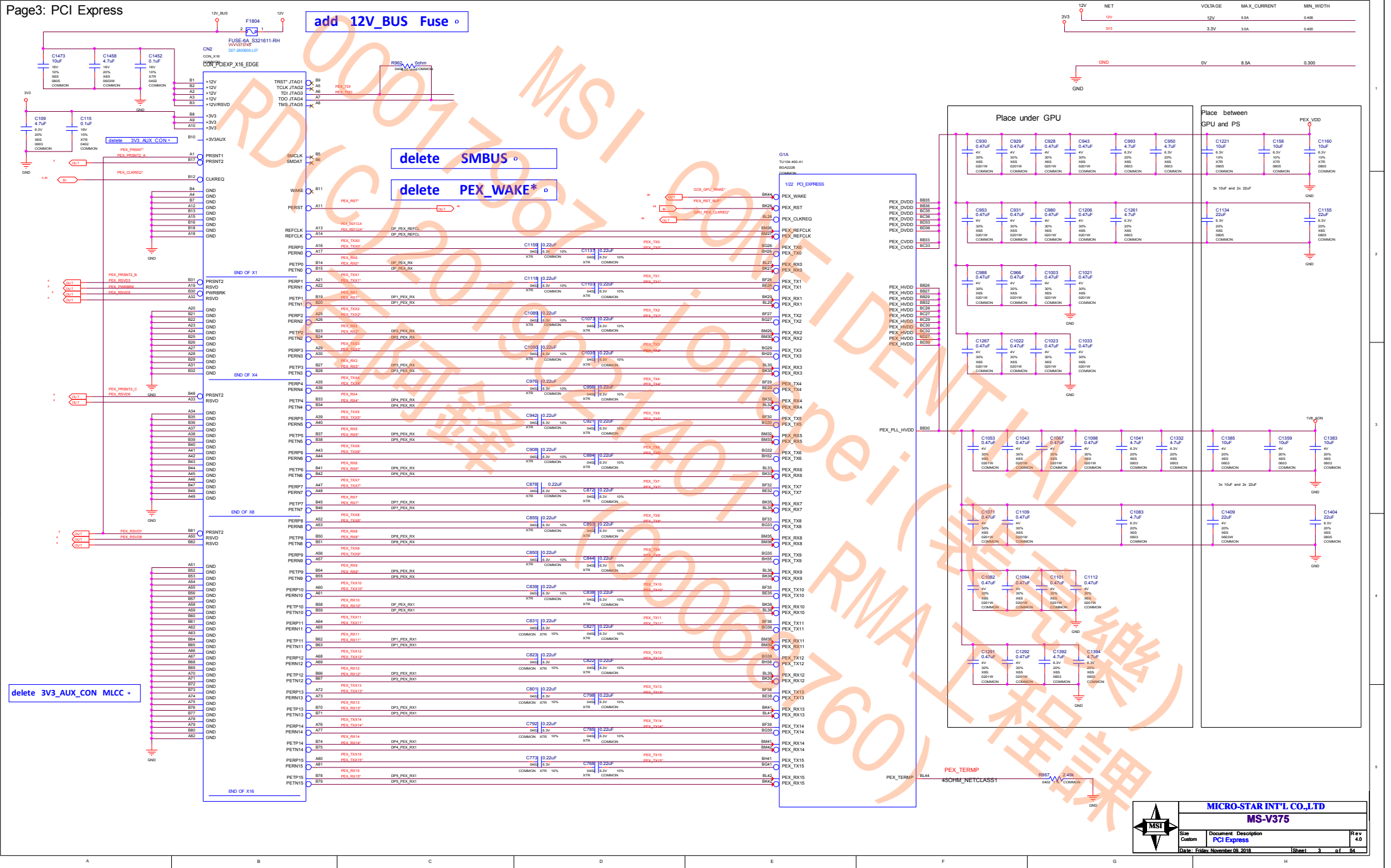
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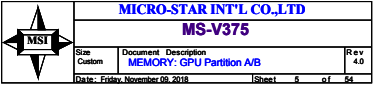
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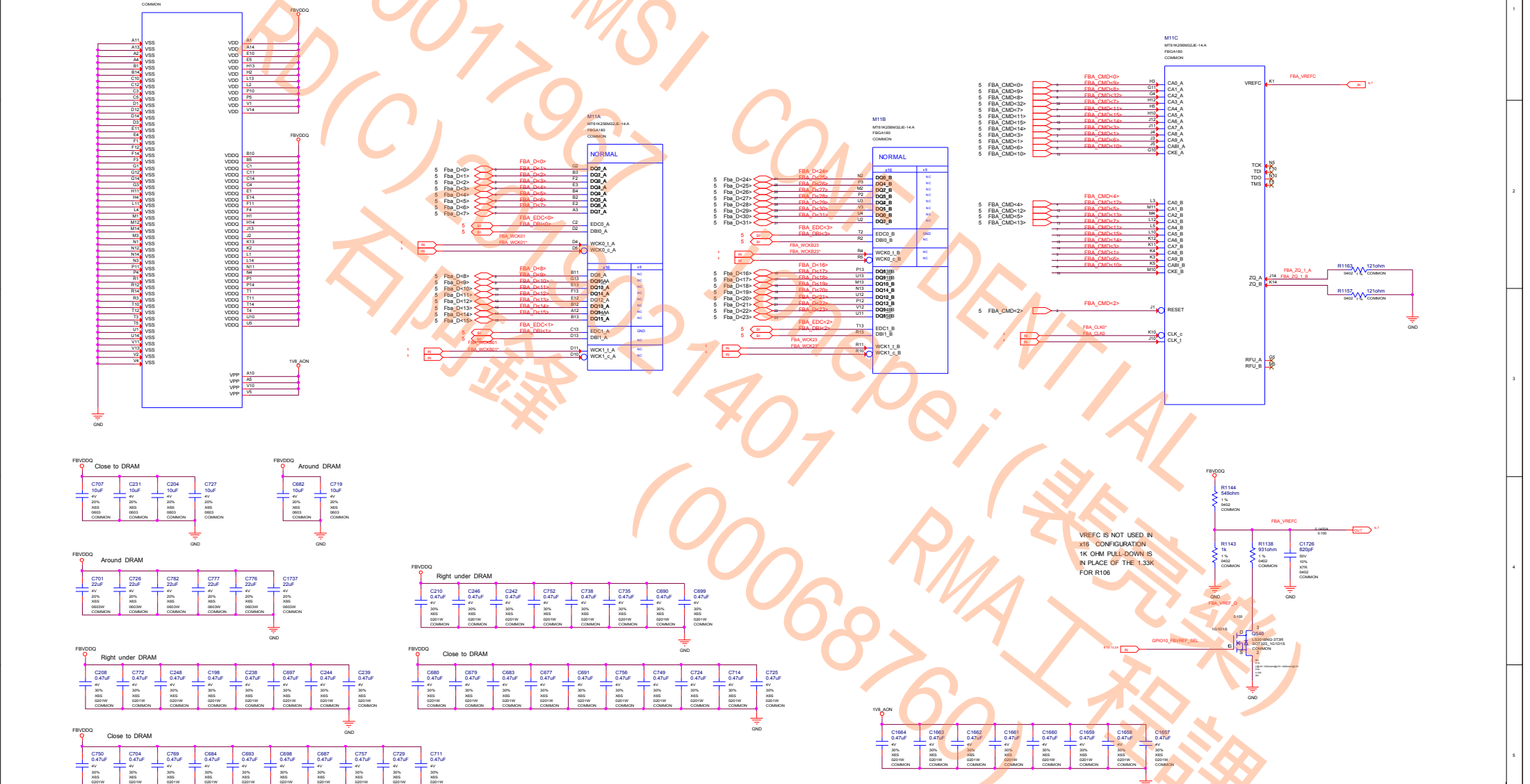
51	MECH
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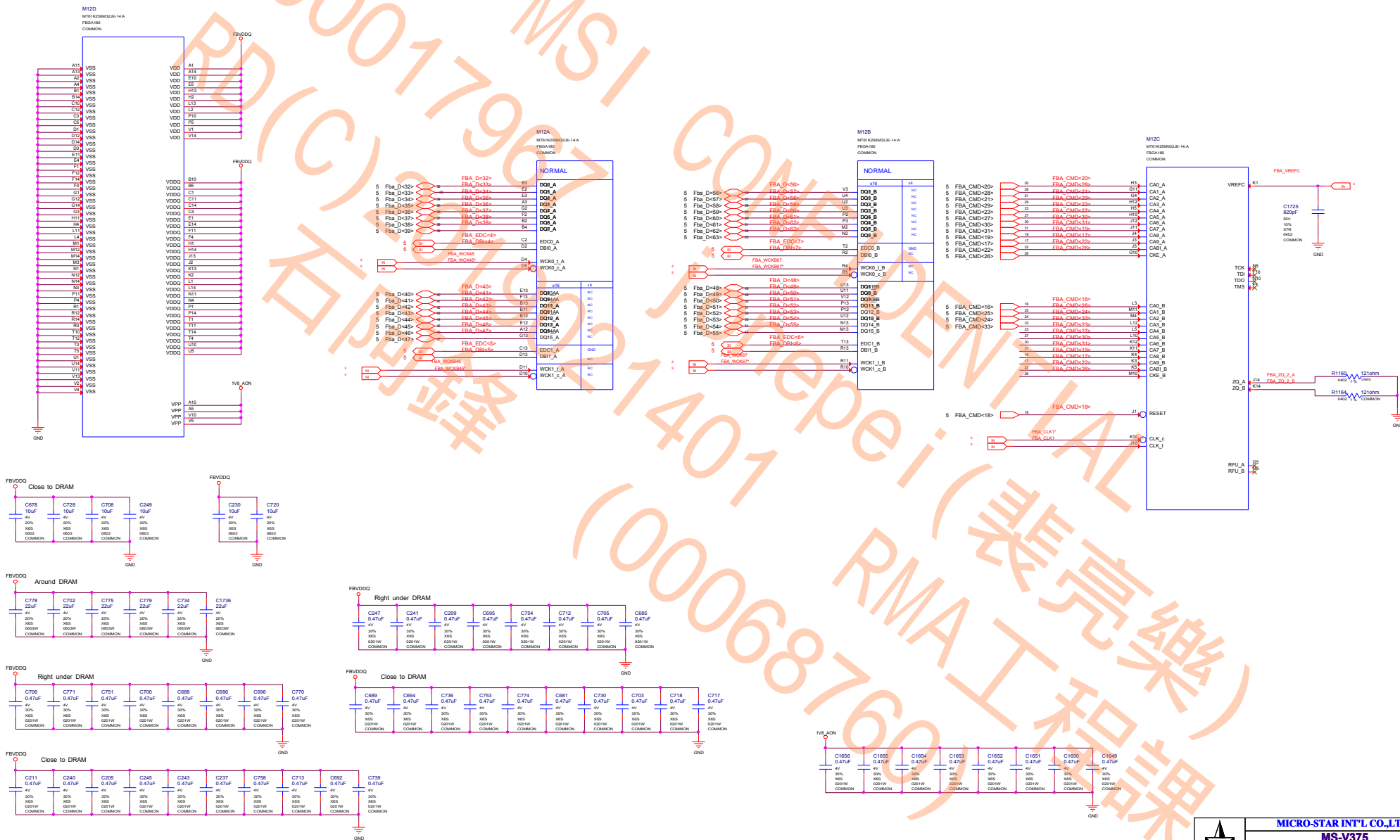
Page2: Block Diagram



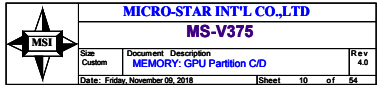


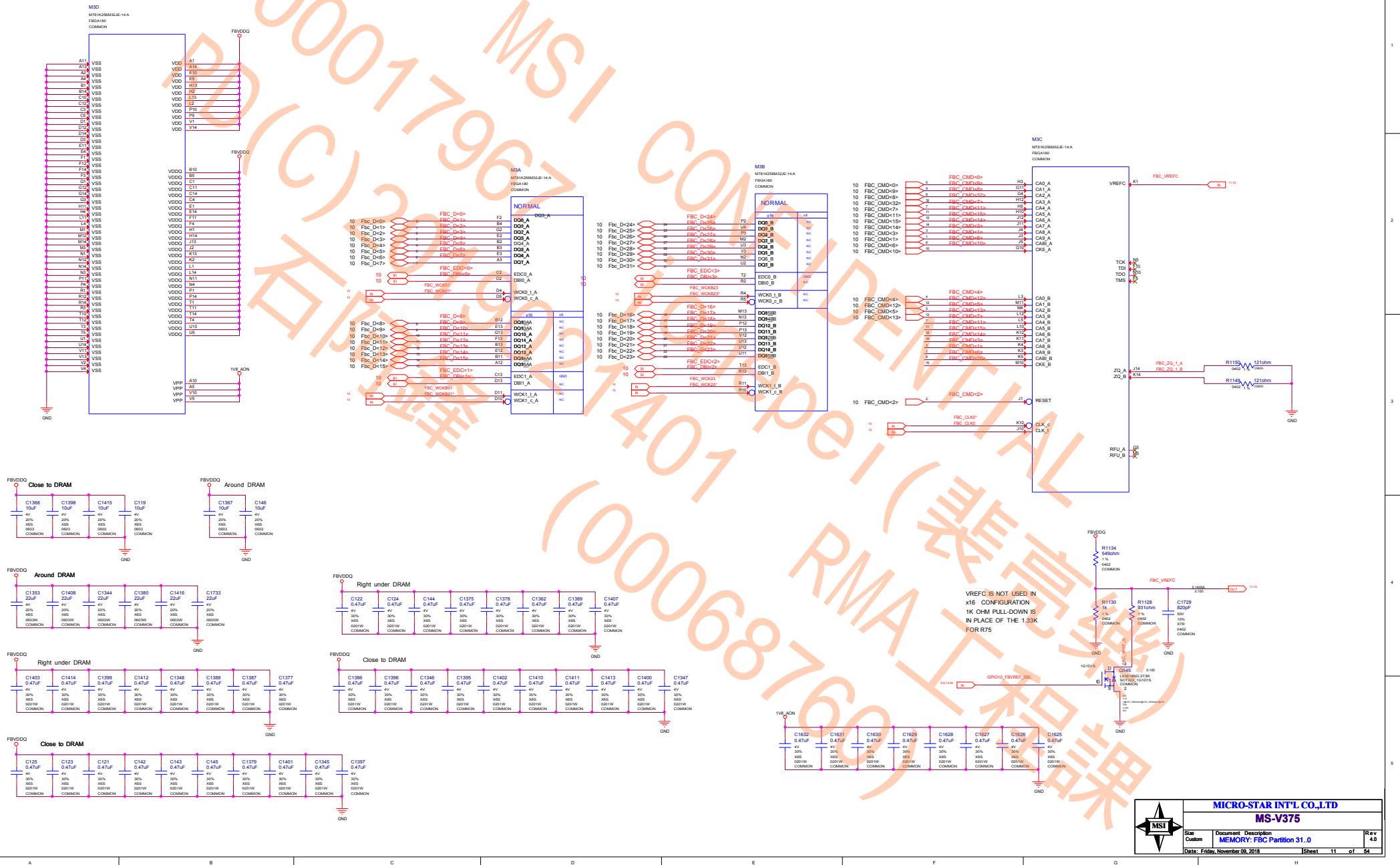


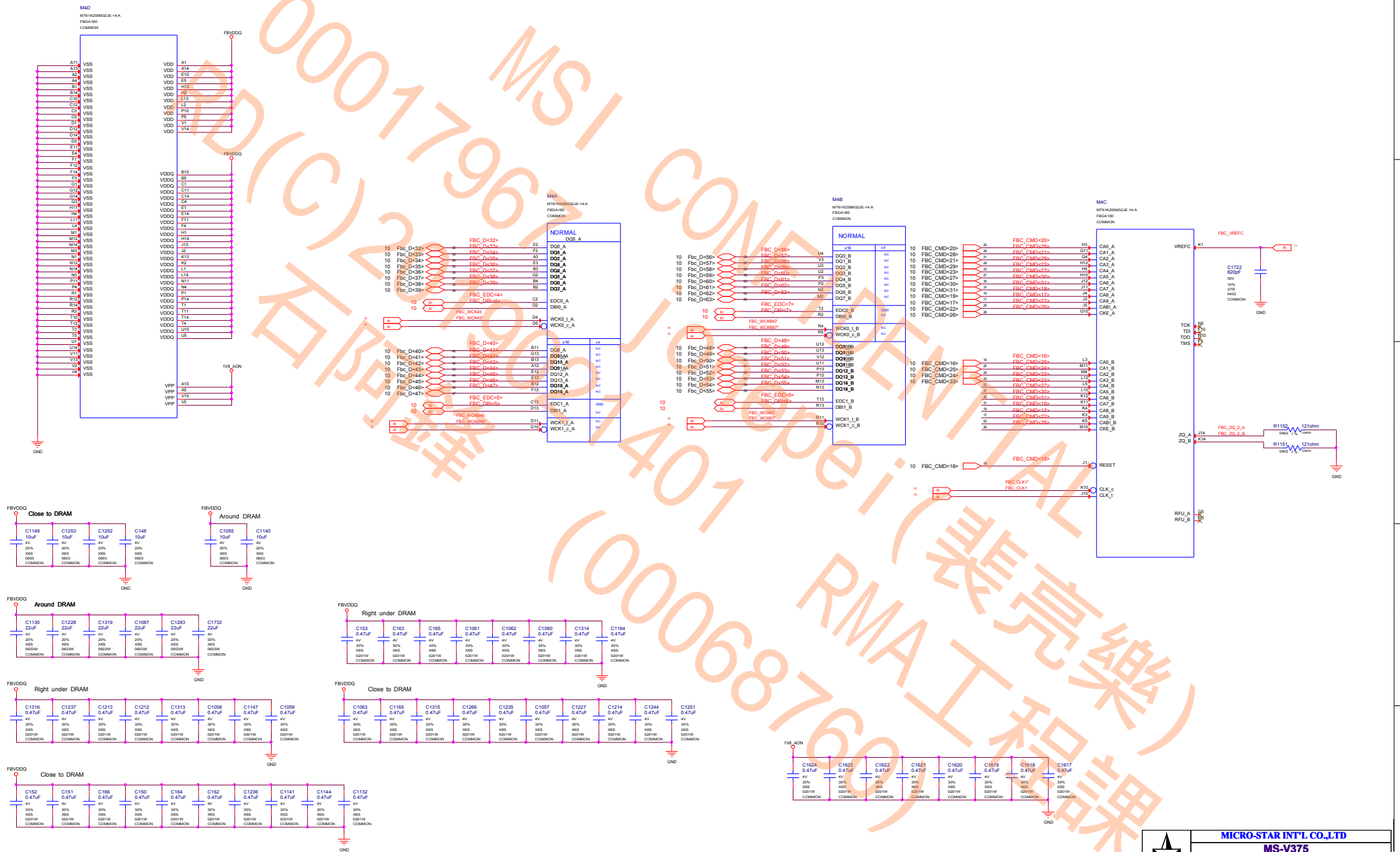


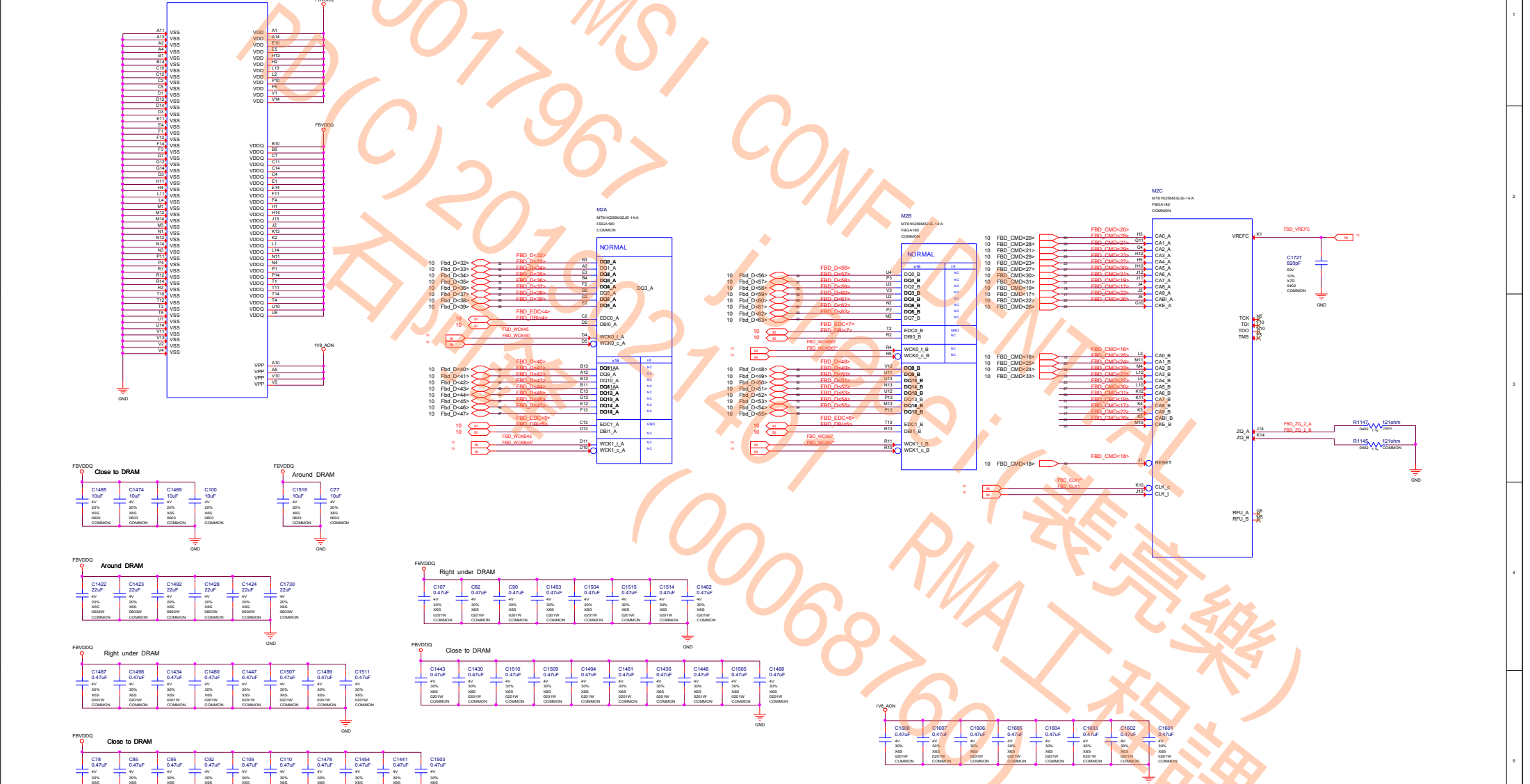








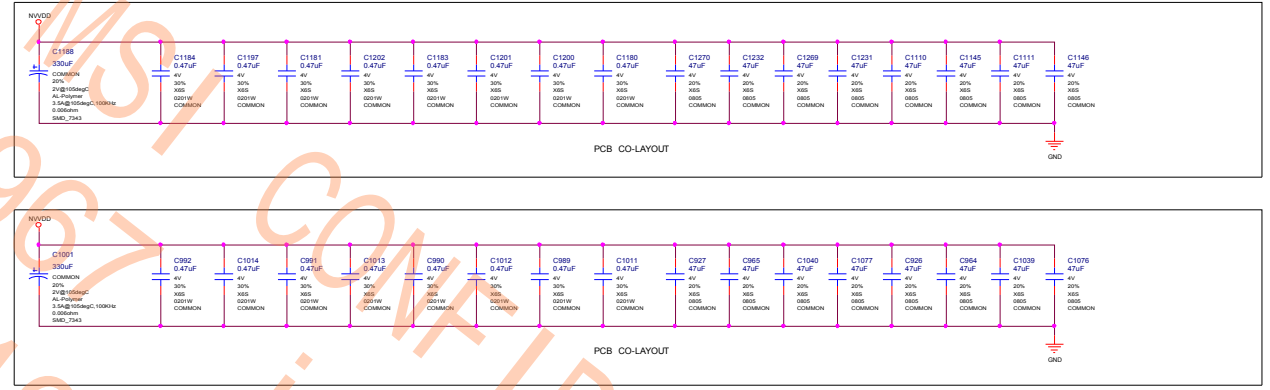




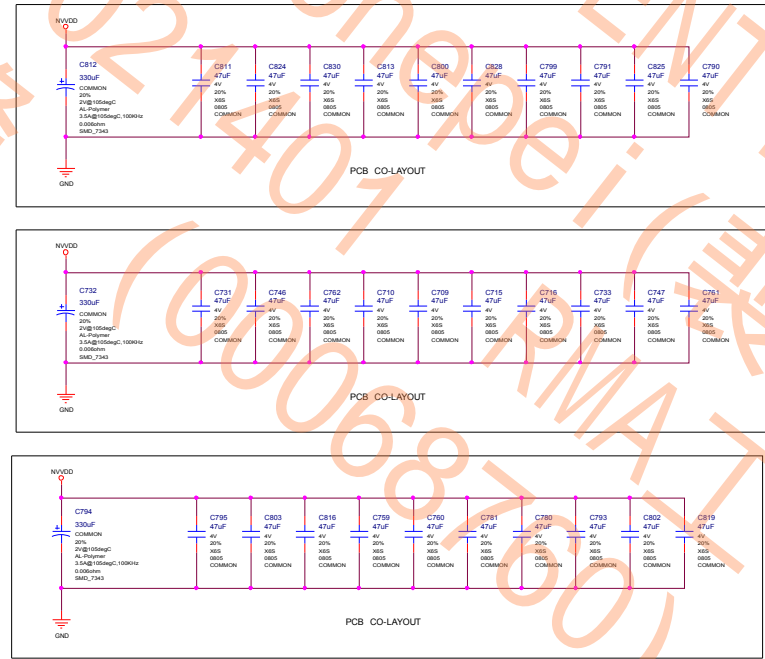
FBVDDQ



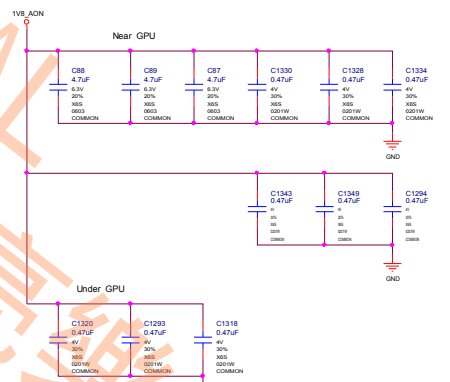
Under GPU

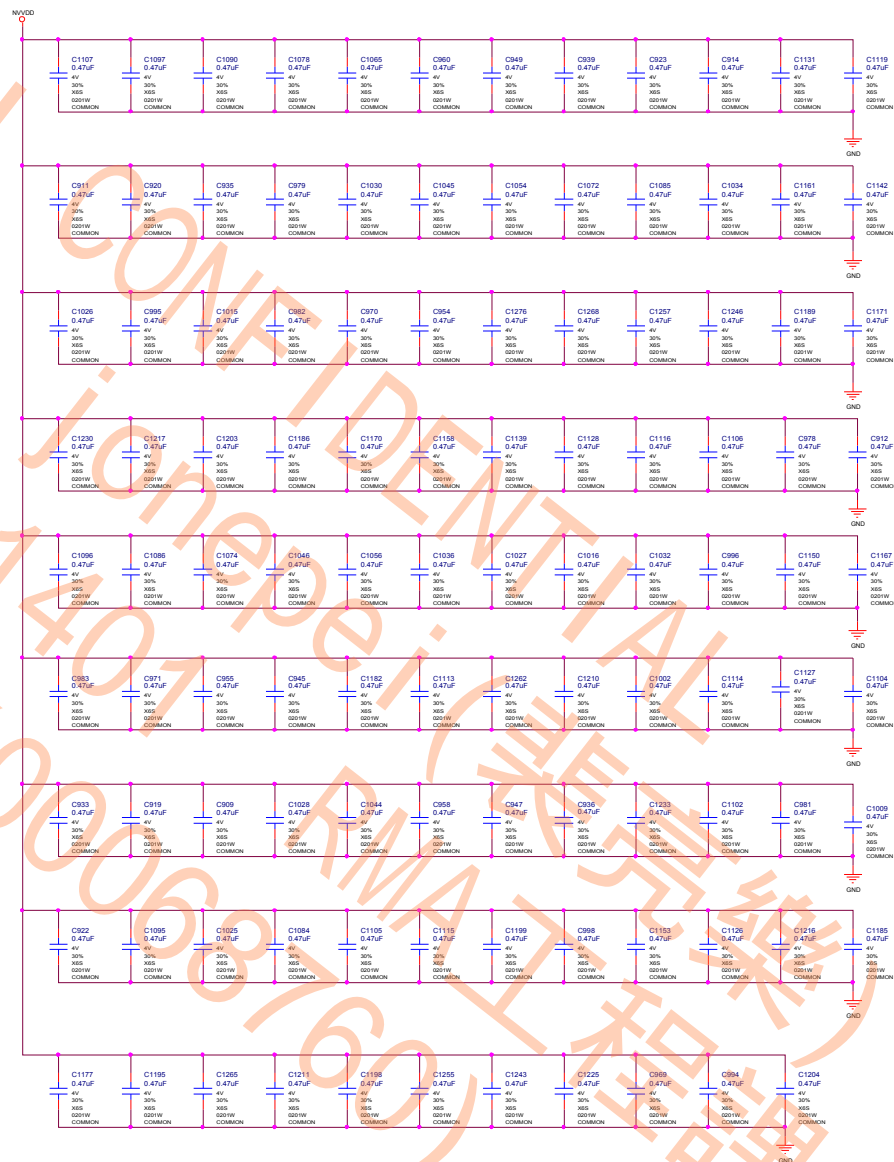


Near GPU



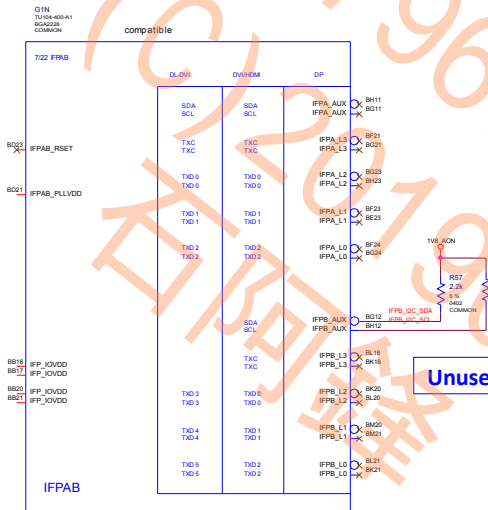
1V8_AON





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[delete Link AB](#)

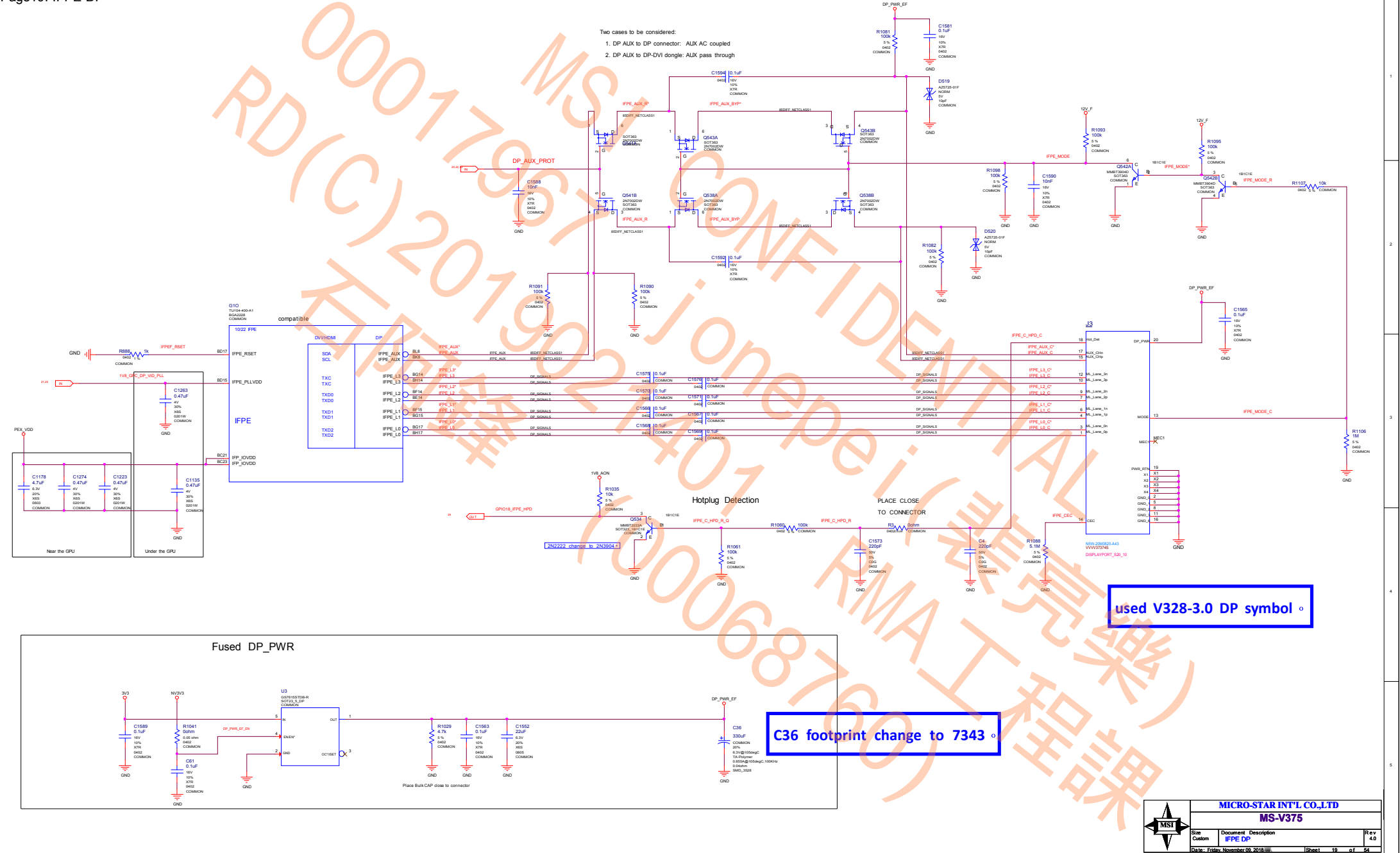


9.3 UNUSED PINS

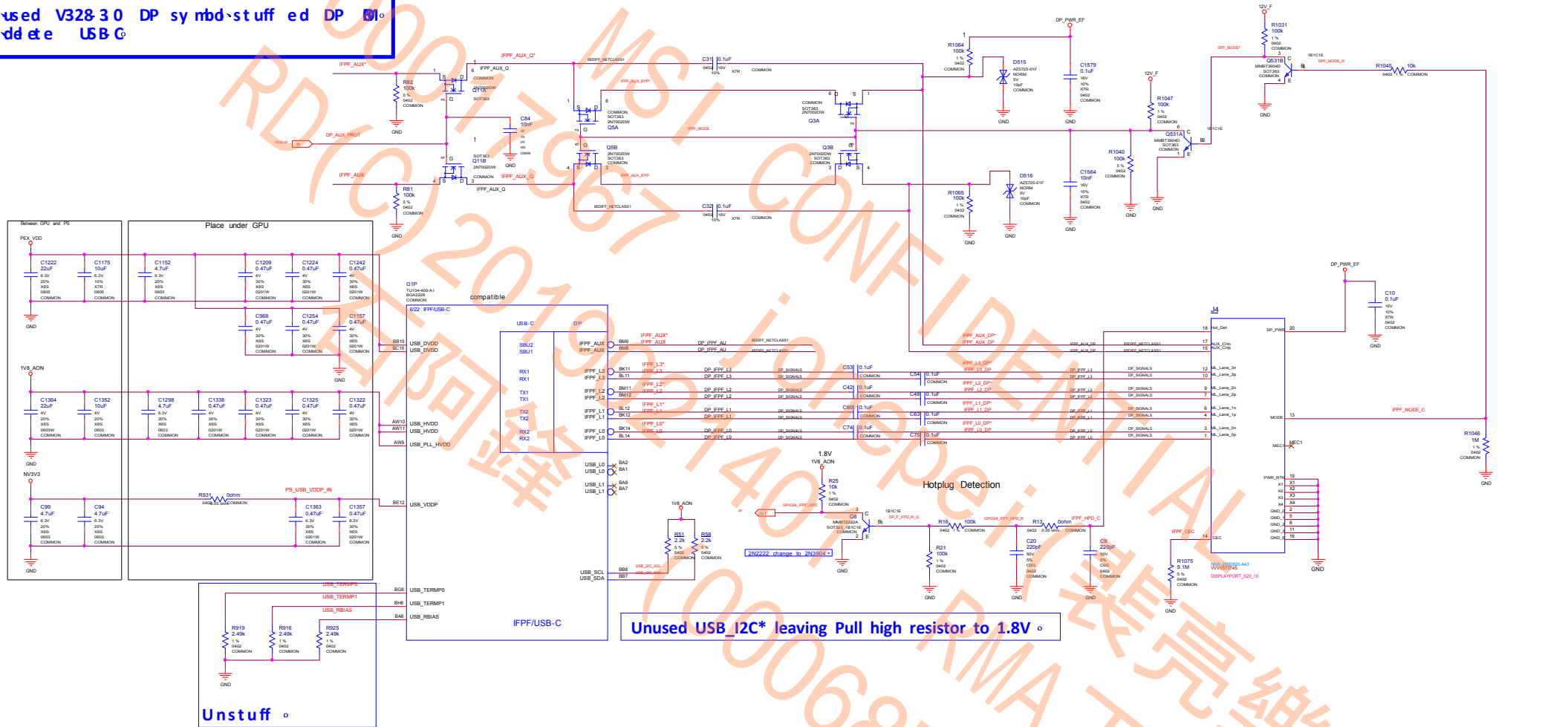
If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF) can be left unconnected if neither of IFPx /IFPy is in use. For example, If neither link of the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD and IFPAB_RSET should be left disconnected, and all signals and references associated with Link A and Link B should also be left unconnected.

IFP_IOVDD rail can be unconnected if no IFP link is used. If any IFP is used, all IFP_IOVDD balls must be connected to power rail.

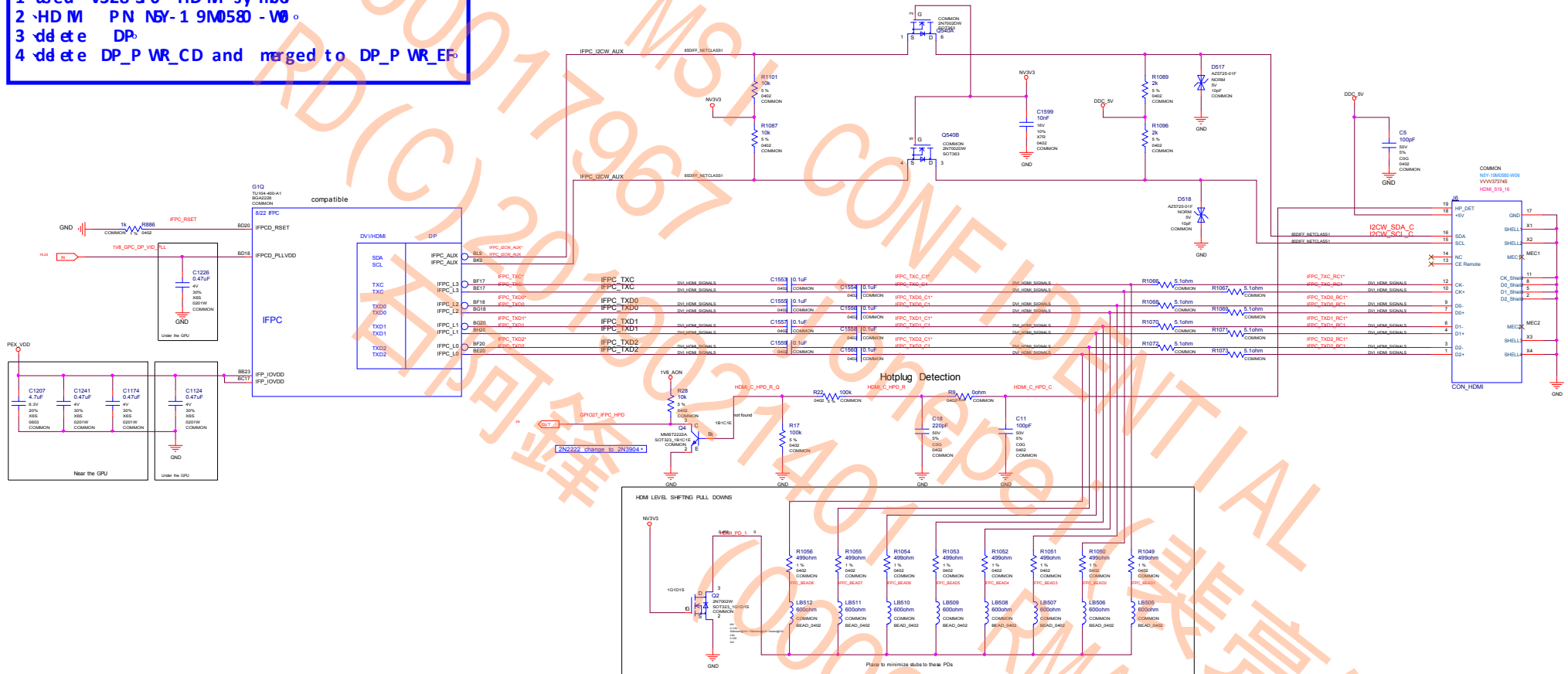
Unused IFPB_I2C* leaving Pull high resistor to 1.8V



1 used V328 3.0 DP symbol stuff ed DP
2 delete USB C



- 1 used V328-3.0 HDMI symbol
- 2 HDMI PIN N5-19M58D - V0
- 3 delete DP
- 4 delete DP_P WR_CD and merged to DP_P WR_EF





STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

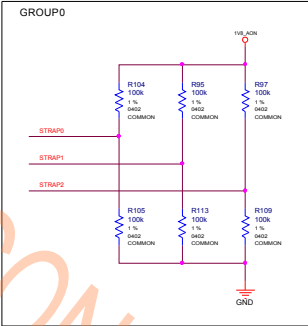
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]	FS_OVERT	1.ENABLE 0.DISABLE	DEFAULT
L	L	L	XXX1		FS_OVERT ENABLE	
L	L	M	XXX0		FS_OVERT DISABLE	

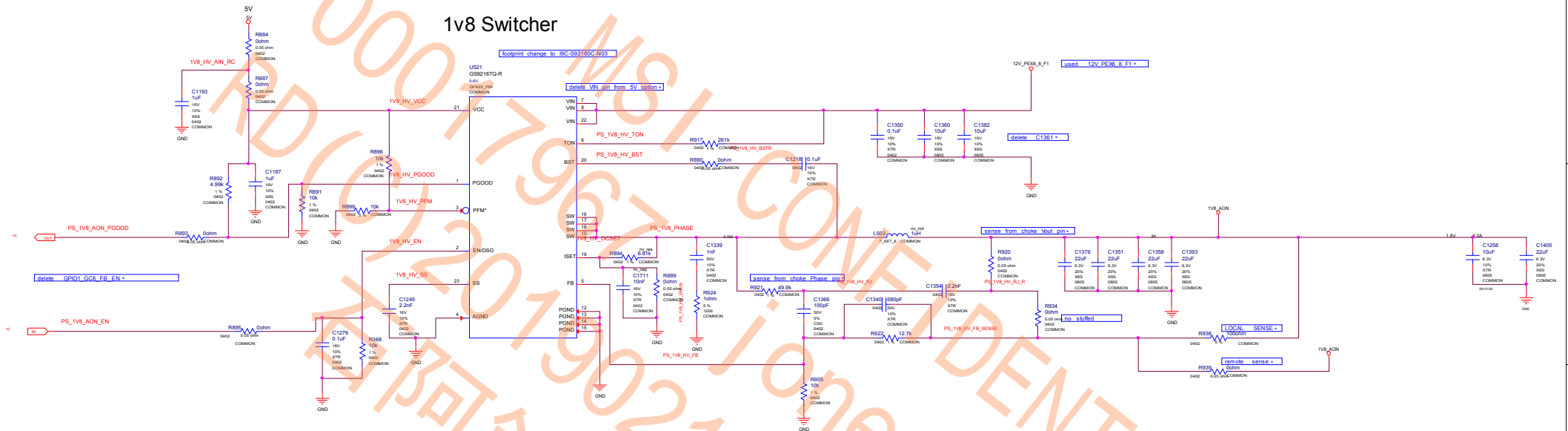
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

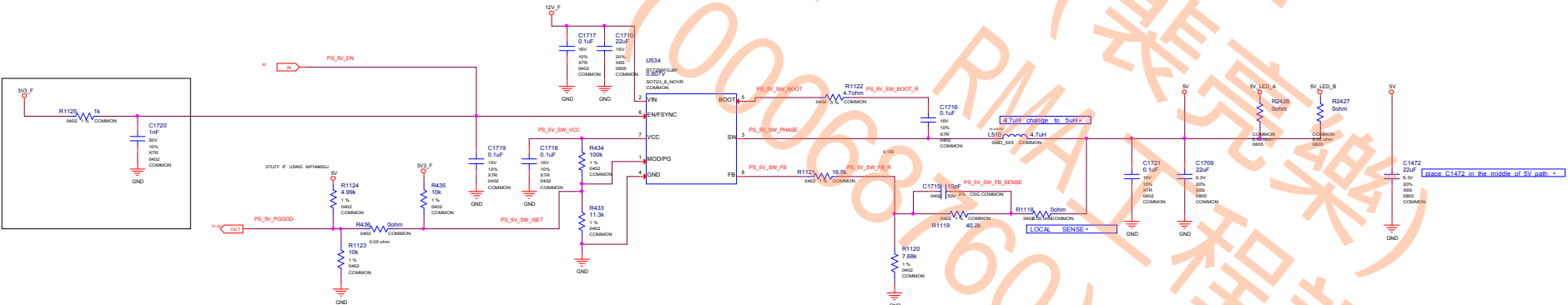
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

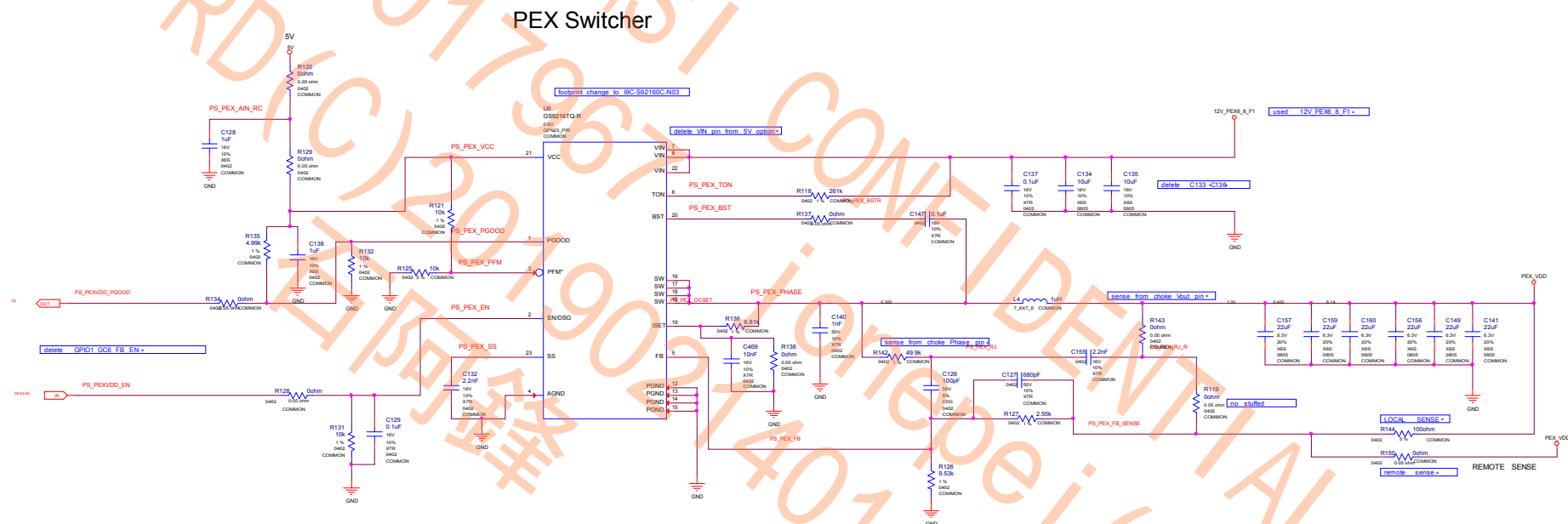




- 1 L503 PNL04-01074K-L65 / footprint : CHK_S2_7_3X6_61
- 2 delete colayout P WM ouput choke
- 3 delete 1V8_MA N and merged to 1V8_AON

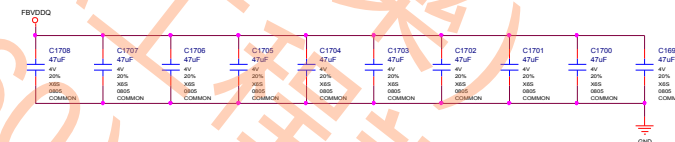
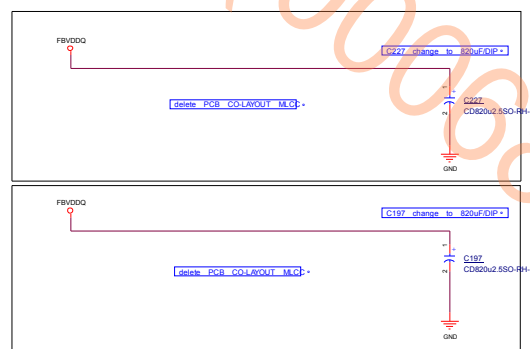
- 1 L510 P N L04-0507010-L65 / footprint : CHK_S2_5_4X5_23
- 2 d d e t e colayout P W M ouput choke
- 3 unused RTD3 d d e t e Buck-Boost regulator

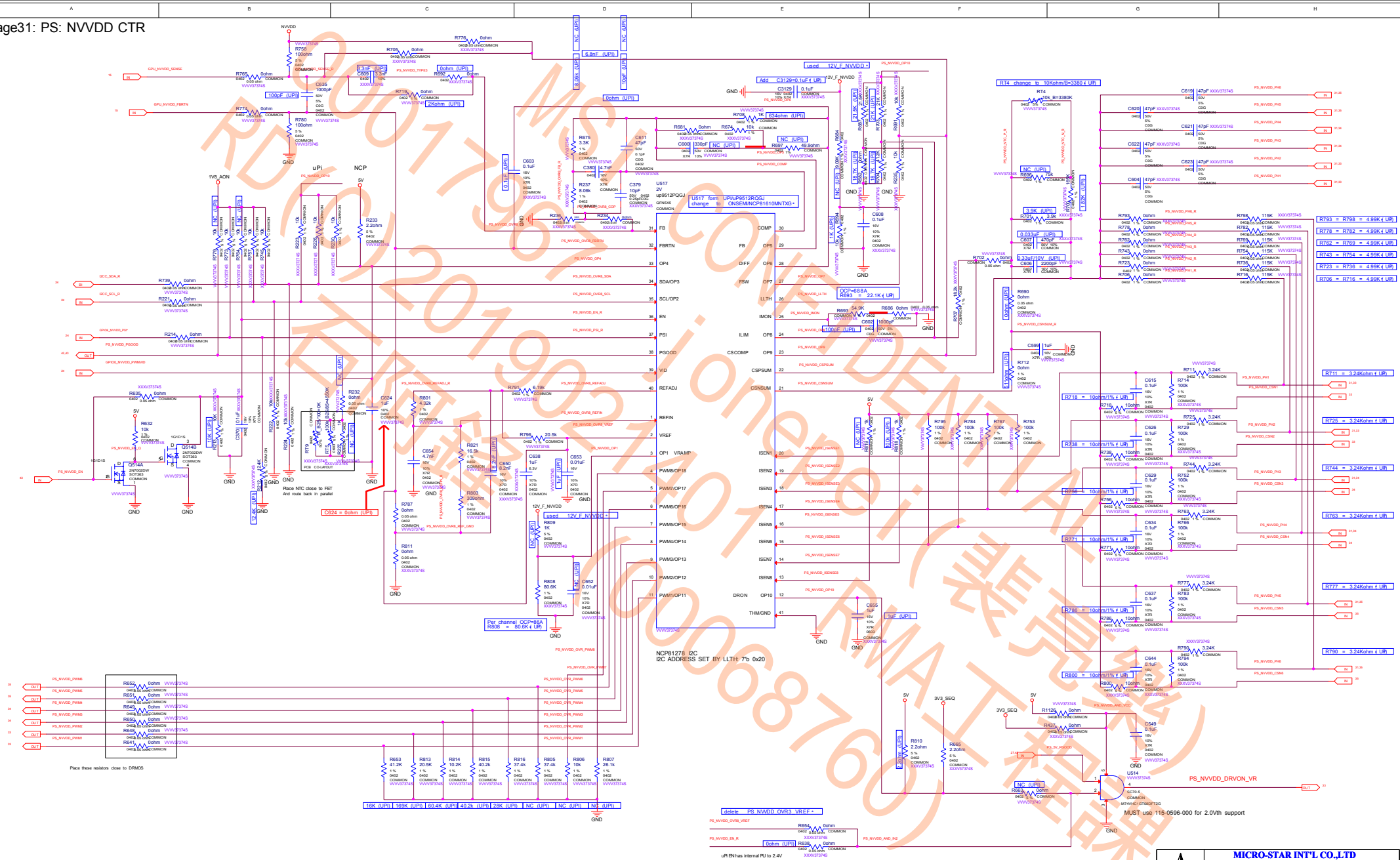




1 L4 PN L04-0107410-L65 / footprint : CHK_S2_7_3X6_61
2 delete colayout P WM ouput choke





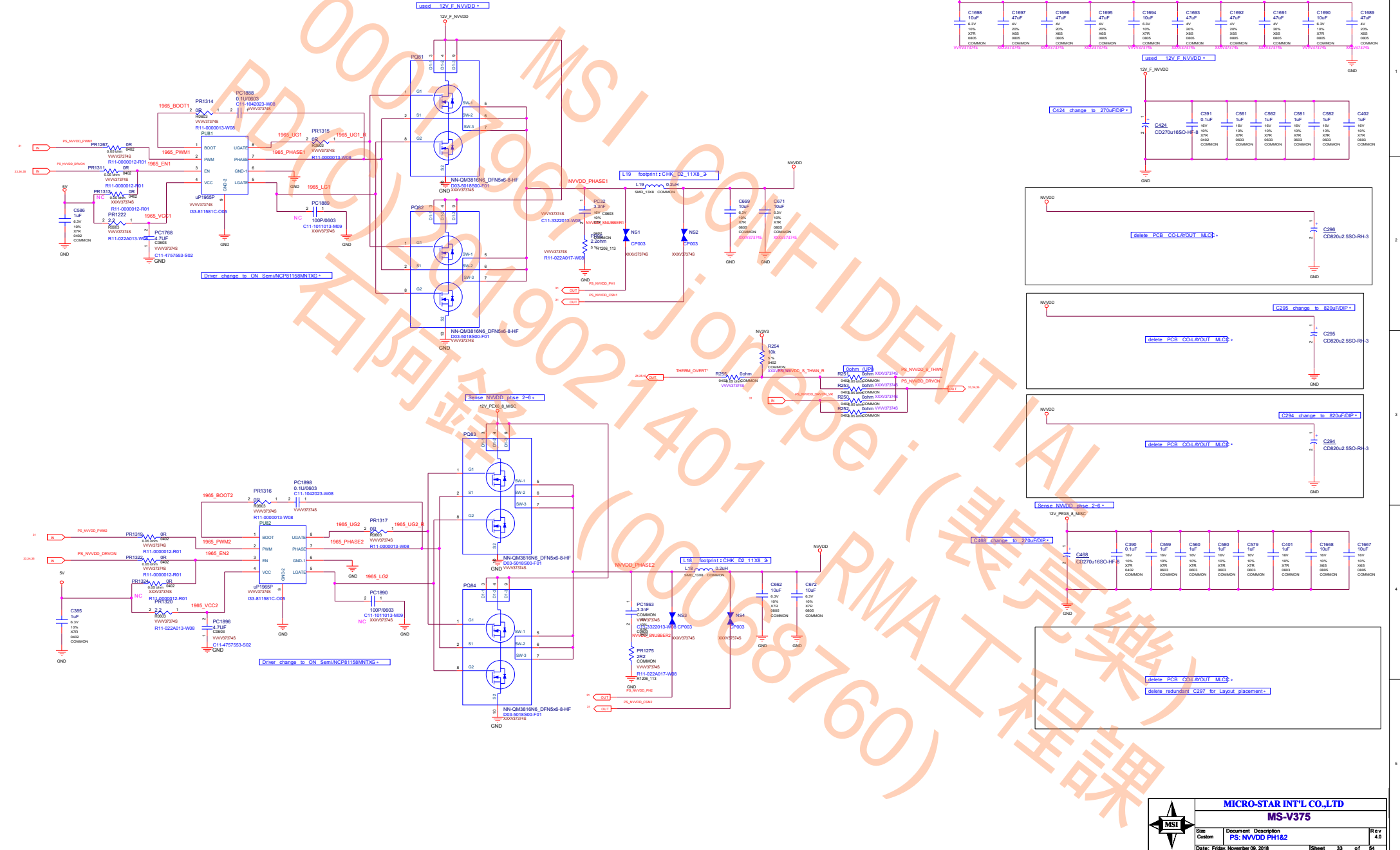


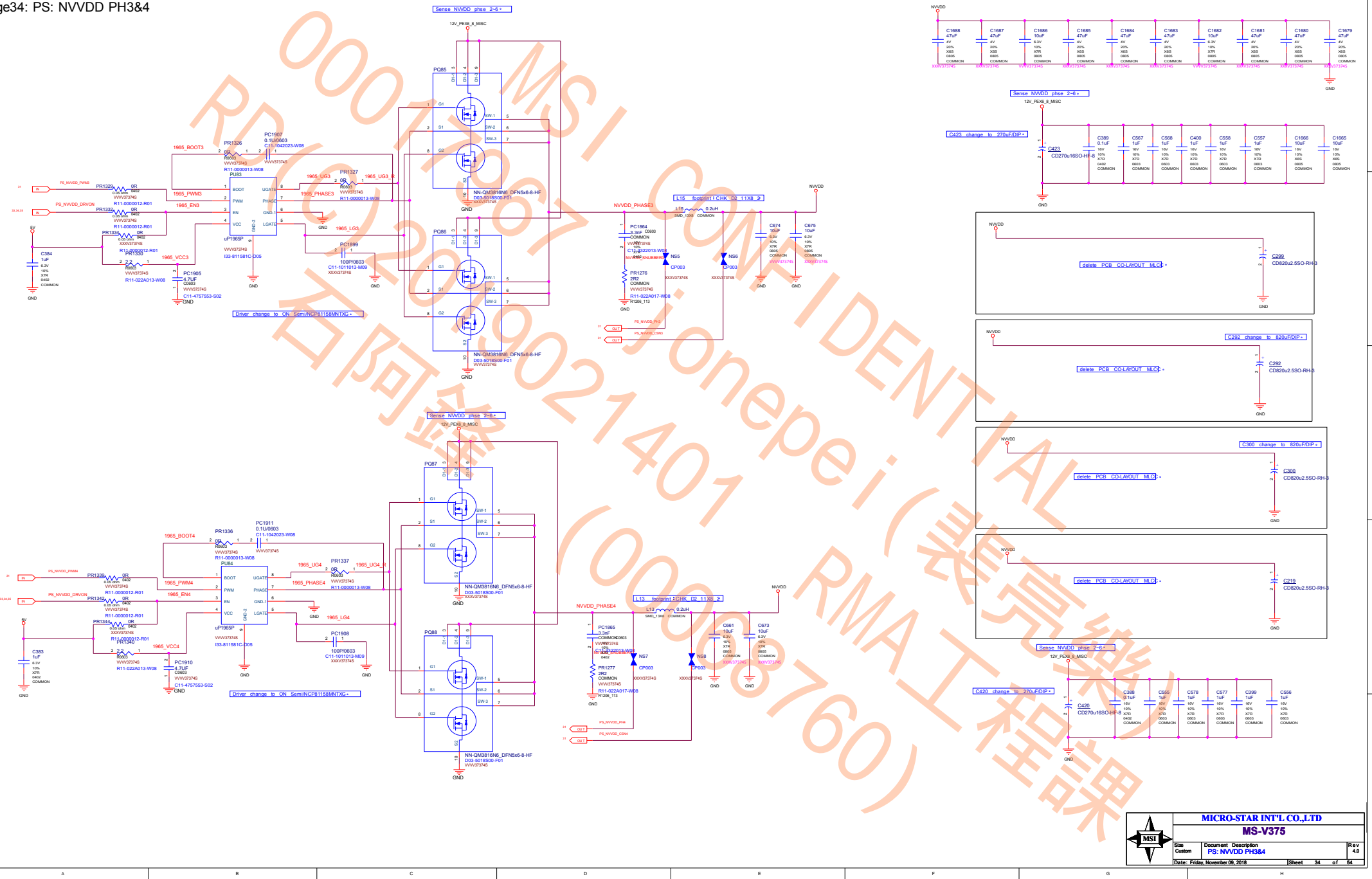
delete all unused

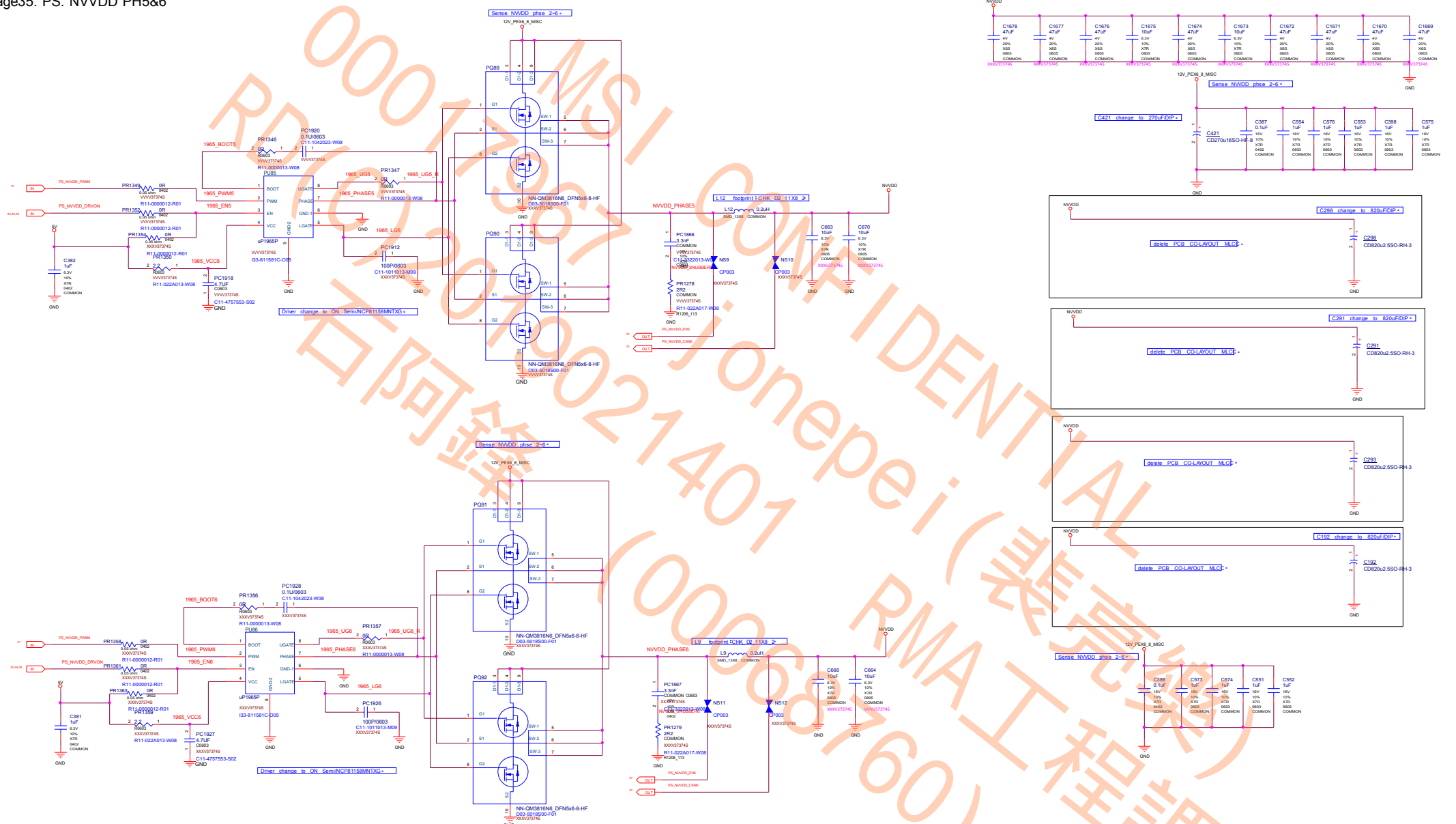
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石阿鋒
jonepei (裴亮樂)
(00068760) RMA工程師



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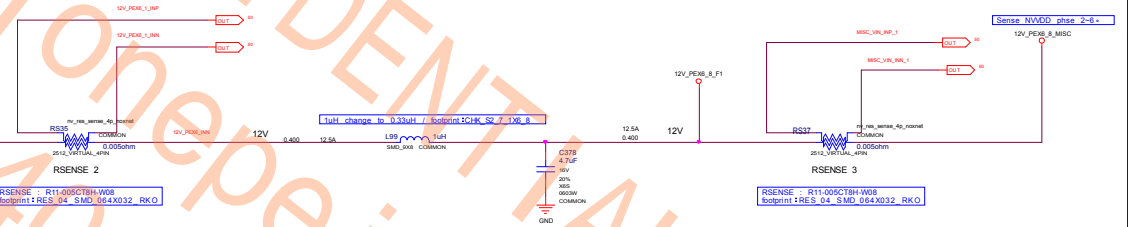
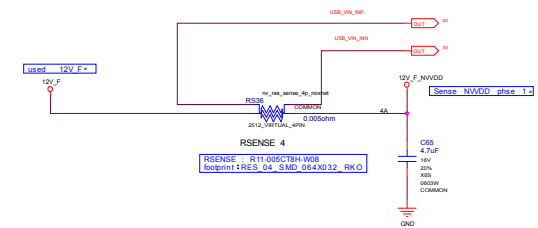
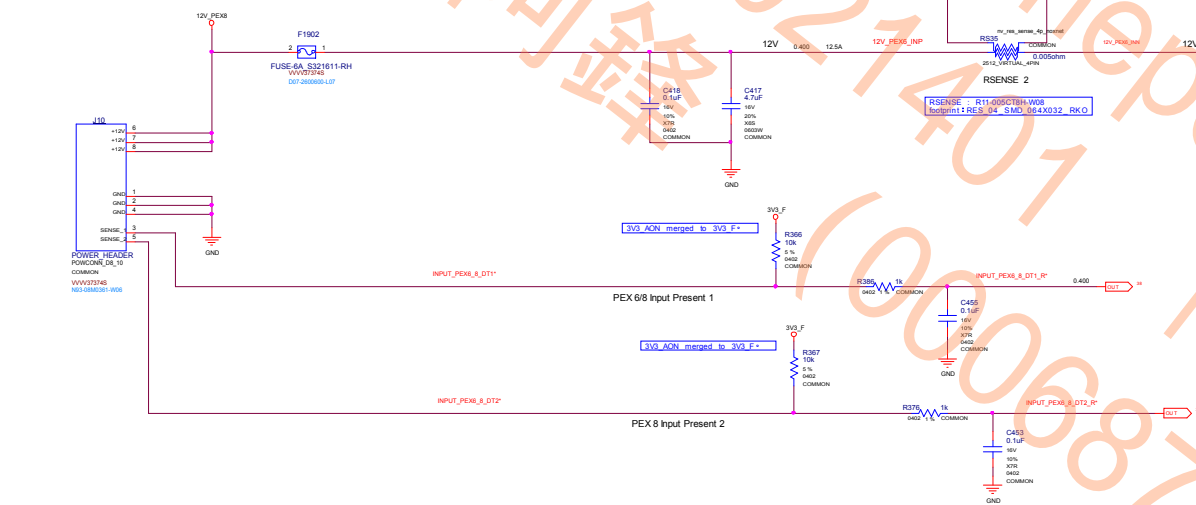
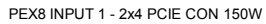
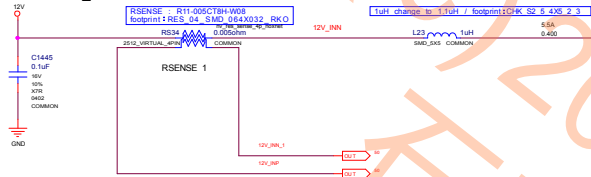
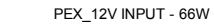
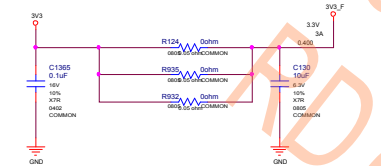
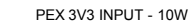




removed U511 for fixed NVVDD 12V input:
1 merged 3V3_AON to 3V3_F
2 unused and delete 3V3_AUX
3 unused and delete 3V3_AUX_CON
4 NVVDD_DYN_V N merged to 12V_PEX6_8_F1

Delete GPOL INPUT DYN BAL1
Delete INPUT PEX6 D11 STEER

- 1 changed EXT 12V 8pin PN and footprint.
- 2 add EXT 12V 8pin Fuse.
- 3 delete unused parts.
- 4 RSENSE 3 change to sense NVVDD PEX 12V.
- 5 RSENSE 4 change to sense NVVDD EXT 12V.
- 6 change RSENSE parts and footprint.



Sense resistors should be located as close as possible to the OVR-M input pins. Otherwise sensor output signals may exhibit larger measurement errors due to additional trace inductance and noise coupling in the signal from nearby noise-generating sections of the board.

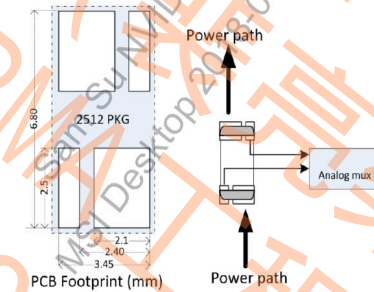


Figure 5.10 Connection for 2-Pin Sense Resistor (2512 Package)

If customer prefers using a 2-pin sense resistor instead, we recommend implementing a 4-pin footprint with two large PADs for the high current path and two small PADs for sensing line, to emulate the functionality of a 4-pin resistor.

Note: Two-pin sense resistor can be used, but the sensing signal **MUST** connect to resistor pad directly. Connect the sensing signal to nearby power plane may cause large measurement error.



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delete regulator for USBC_VBUS °

Unused USB_I2C* leaving Pull high resistor to 1.8V °

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delete PPC ◦

Unused USB_I2C* leaving Pull high resistor to 1.8V ◦

Unused IFPB_I2C* leaving Pull high resistor to 1.8V ◦

delete GPIO4_IPPB_HPD ◦

delete PEX_RST_BUF* ◦

delete GPIO1_GCS_FB_EN* ◦

unused and delete all °

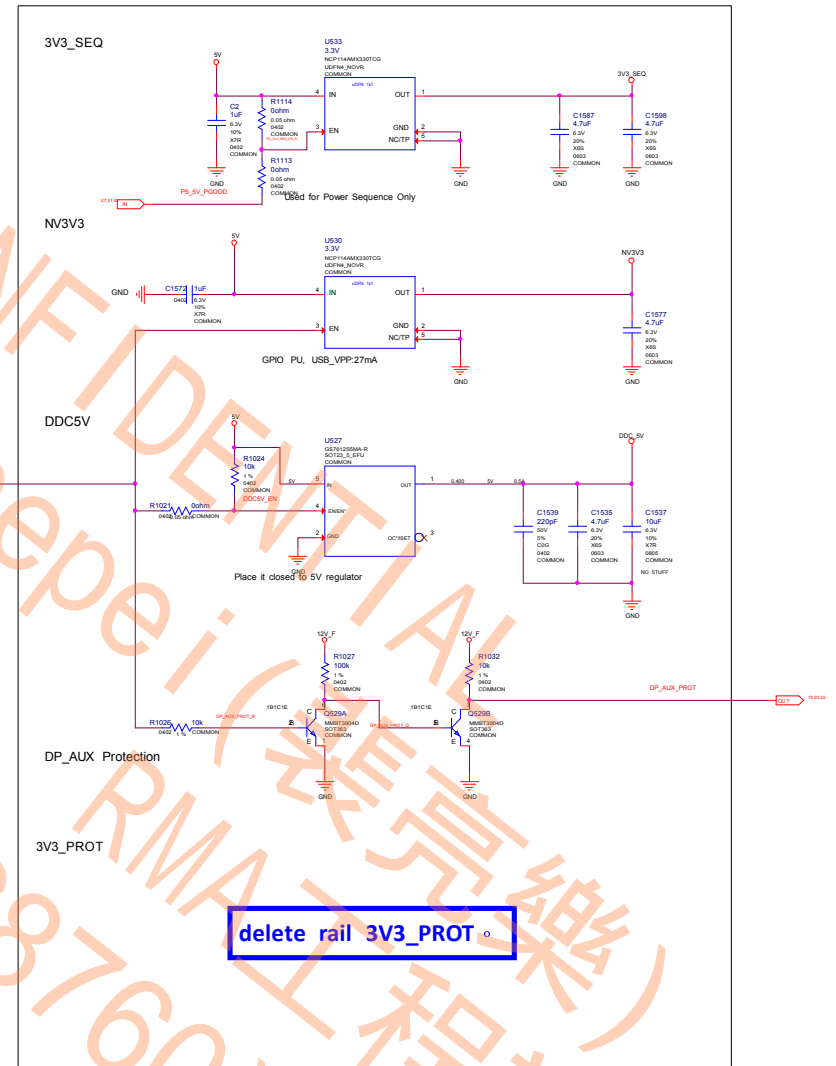
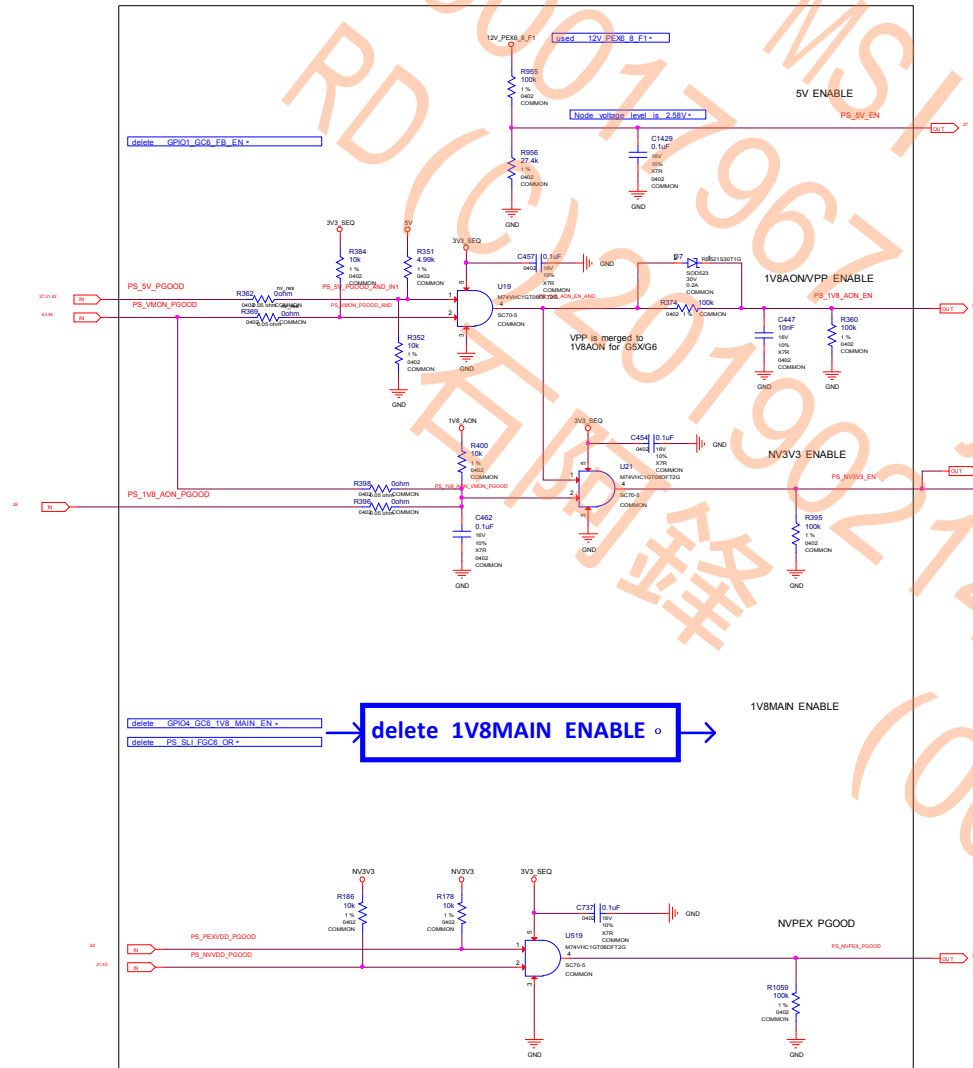
delete _GP001_GCE_FB_EN+
delete _GP002_DVE_IN_SW1

delete _offpage_PPS_BTD_SWITCH

unused and delete GP004



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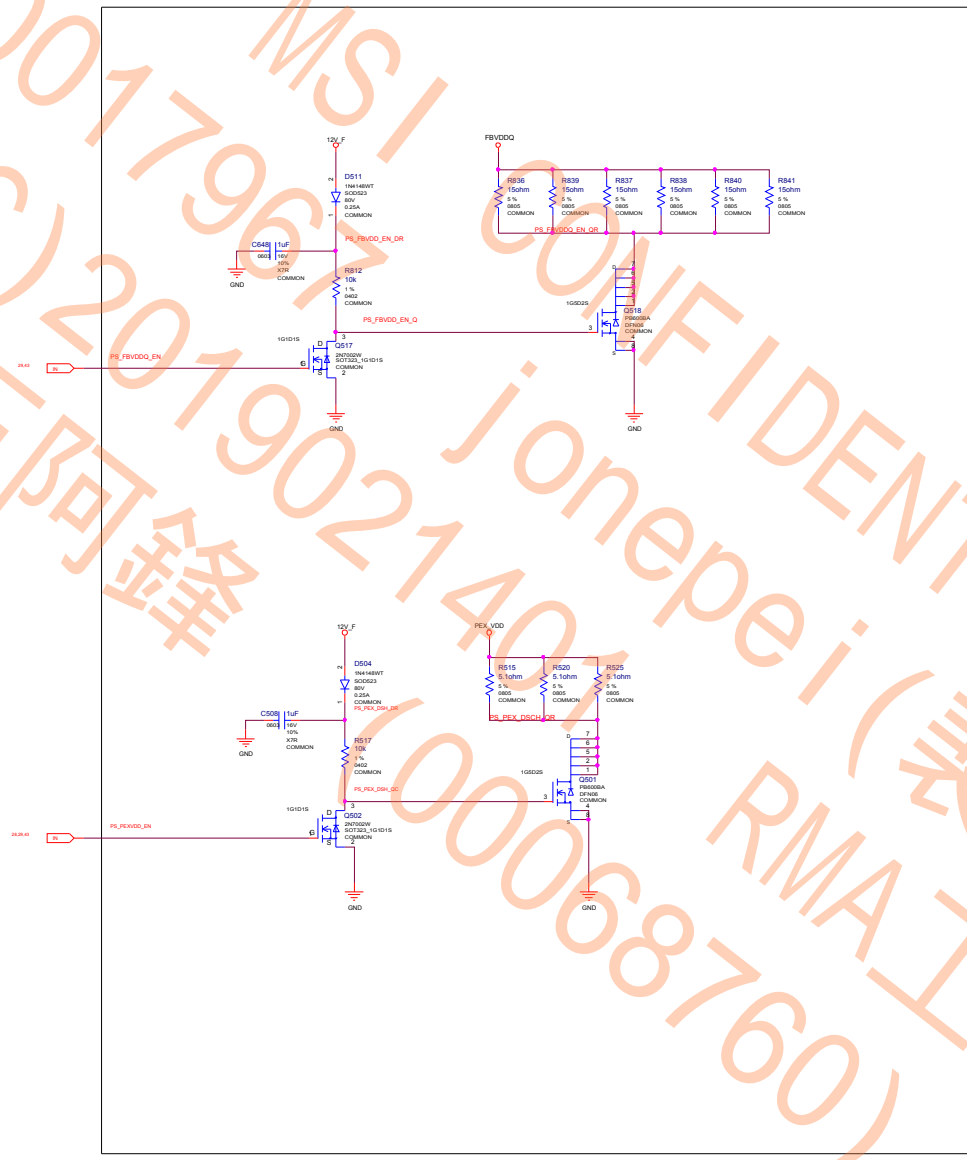


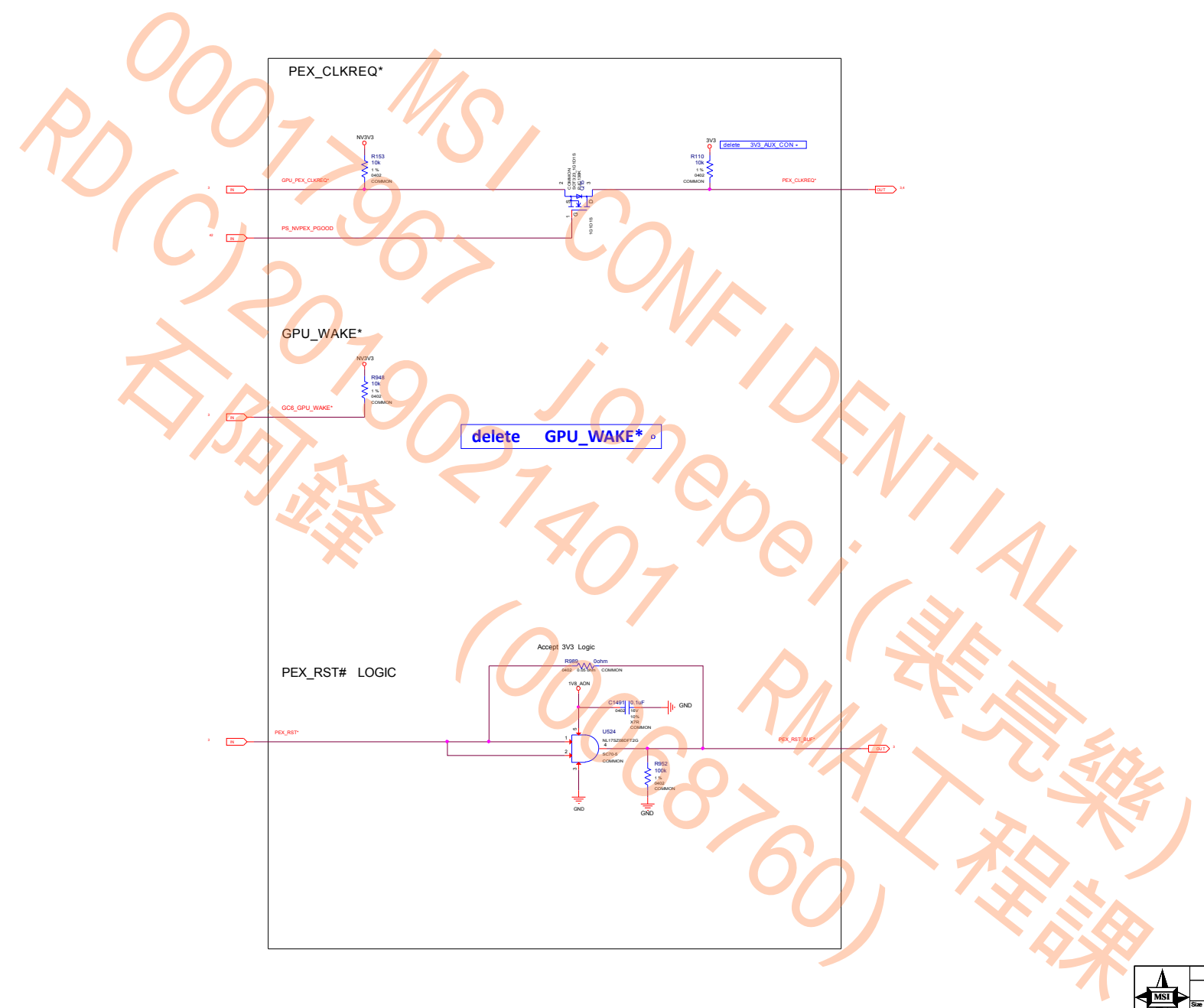


OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGGOOD	OPEN-DRAIN	Floating(?) once both 3V3 and 12v reach Vth
G06_FB_EN	INPUT	Indicator for RTD3/G06 residence, Use to Mask the VMON_PGGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSKOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)







delete all unused

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delete all unused

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improved FBVDDQ PSU parts don't require a PTC

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